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**Rev. 0.10 [G]**

**2025-03-19**

**Preliminary version**

**TCC805x** **Hardware**

**Application Note**

**For Telechips PMIC Design**

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# Introduction

This document describes the design guide for Telechips Power Management Integrated Circuits (PMIC) applied to TCC805x and summarizes the test results on the TCC805x Evaluation Board (EVB).

# Design Guide for TCC805x EVB

The TCC805x EVB is designed by using TCC5340.

## Telechips Components Information

### Brief Specification of TCC5340

The TCC5340 is a highly integrated, multi-configurable power converter designed to provide functional safety. This device features dual multi-configurable synchronous buck converters and two LDOs, making it ideal for powering safety-related SoCs and application-specific integrated circuit chips (ASICs).

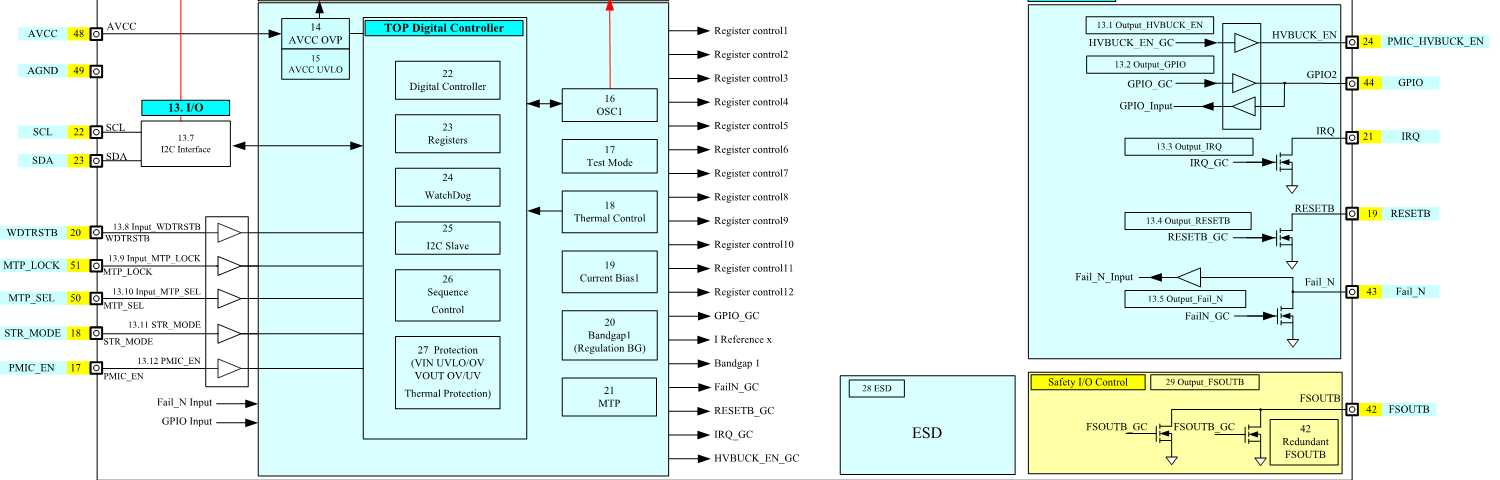
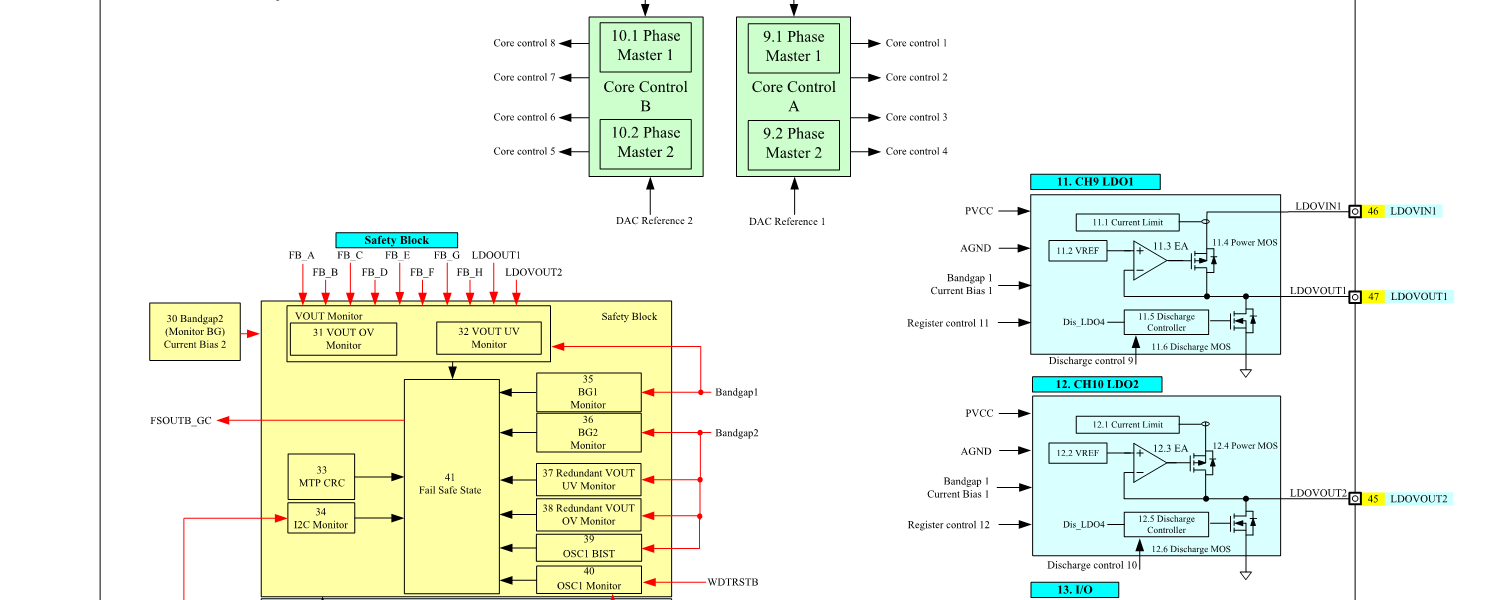
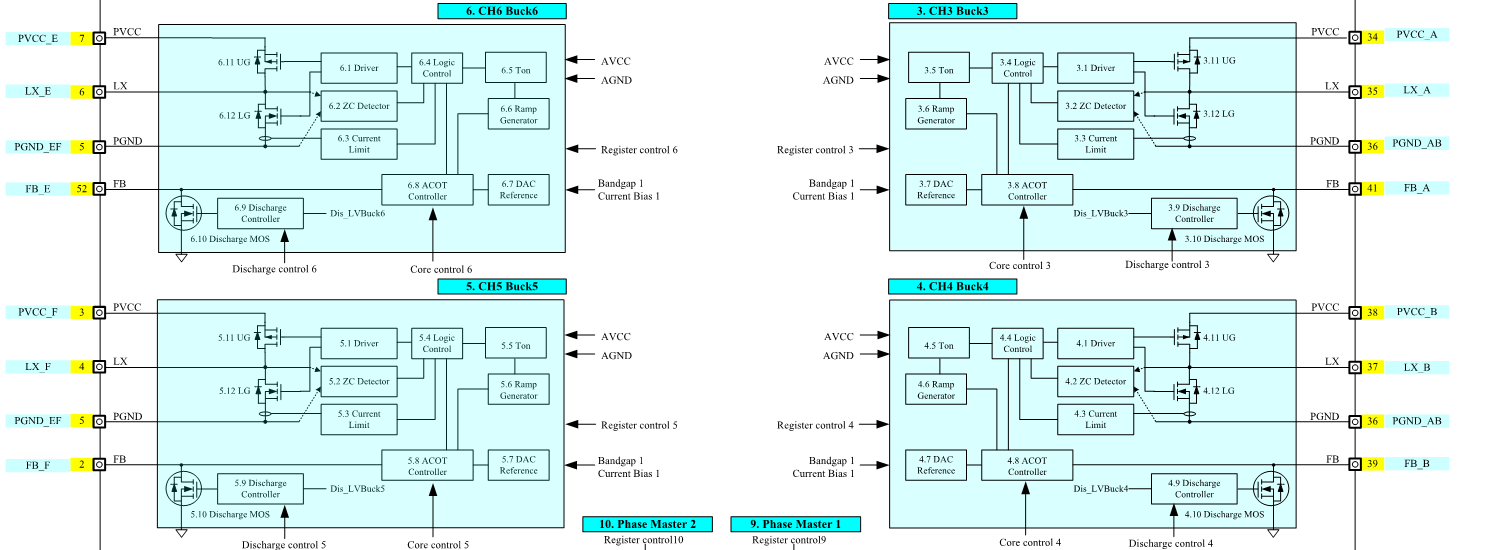
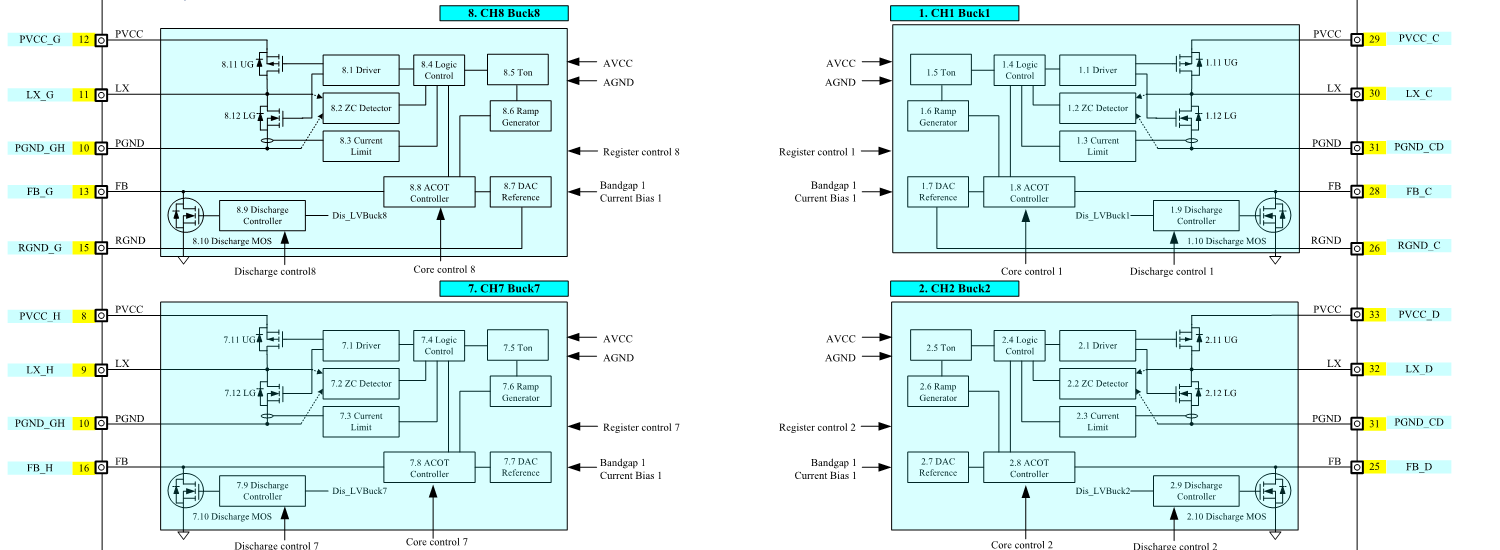


Figure . Block Diagram of TCC5340

#### Features

* Complies with ISO26262 ASIL-B
* AEC-Q100 Grade 1 qualified
* Integrated 8-channel buck converter and 2-channel LDO
* Dual multi-configurable buck converter with 4+0/3+1/2+2/2+1+1 configuration
* Input supply voltage: 3.6V to 5.5V
* 50 μA IQ in STR mode with BUCK\_E and LDO1/2 Alive
* I2C programmable buck output voltage: 0.4V to 2.05V with typical switching frequency of 2 MHz
* Supports 3.3V and 1A output with typical switching frequency of 400 kHz on BUCK\_A and BUCK\_E
* Selectable LDO output voltage range
* LDO1: fixed to 1.2V, 1.8V, or 3.3V
* LDO2: fixed to 0.9V, 1.2V, 1.8V, or 3.3V
* LDO1 and LDO2 support 3.3V and 1.8V Dynamic Voltage scaling (DVS) through I2C
* Differential remote sense feedback for high accuracy
* Programmable soft-start and DVS slew rate
* Configurable rail sequence and default boot-up voltage stored in non-volatile memory (NVM)
* Power good and fail-safe indicators, windowed watchdog and watchdog reset function to prevent system hang
* Input OVLO/UVLO, Output OVP/UVP, thermal shutdown protection, and cycle-by-cycle current limit

#### TCC5340: Duty Limitation of Single-Phase Peak Current for BUCK

The duty limitation of the peak output current depends on the continuous output current (Idc) and the duty of peak current.

The single phase of TCC5340 is recommended to supply up to 5A peak for 50 ms.

* Condition: Vin 4V

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **base lout (A)** | **Ta (°C)** | **peak from base Iout (A)** | **Max peak Iout (A)** | **Period (ms)** | **peak (ms)** | **duty** | **lavg (A)** | **Tj (°C)** |
| 3.2 | 85 | 0 | 3.2 | 100 | 100 | 1 | 3.2 | 137 |
| 3.2 | 85 | 1.8 | 5 | 100 | 100 | 0.1 | 3.38 | 141 |
| 3.2 | 85 | 1.8 | 5 | 100 | 50 | 0.5 | 4.1 | 145 |

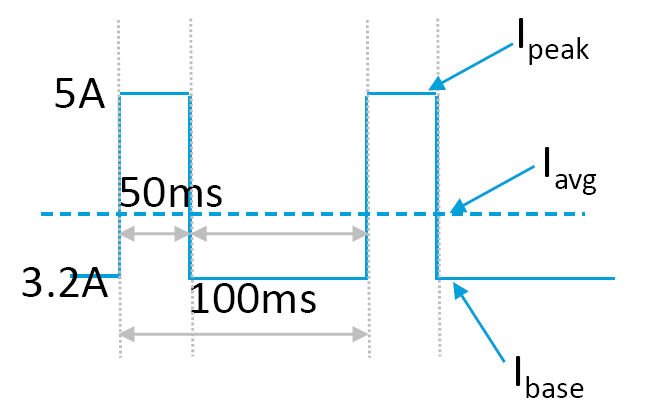


Figure . Waveform of Peak Current Duty (Single Phase)

## Block Diagram of PMICs Power Circuit

Figure 2.3shows the block diagram of PMICs power circuit

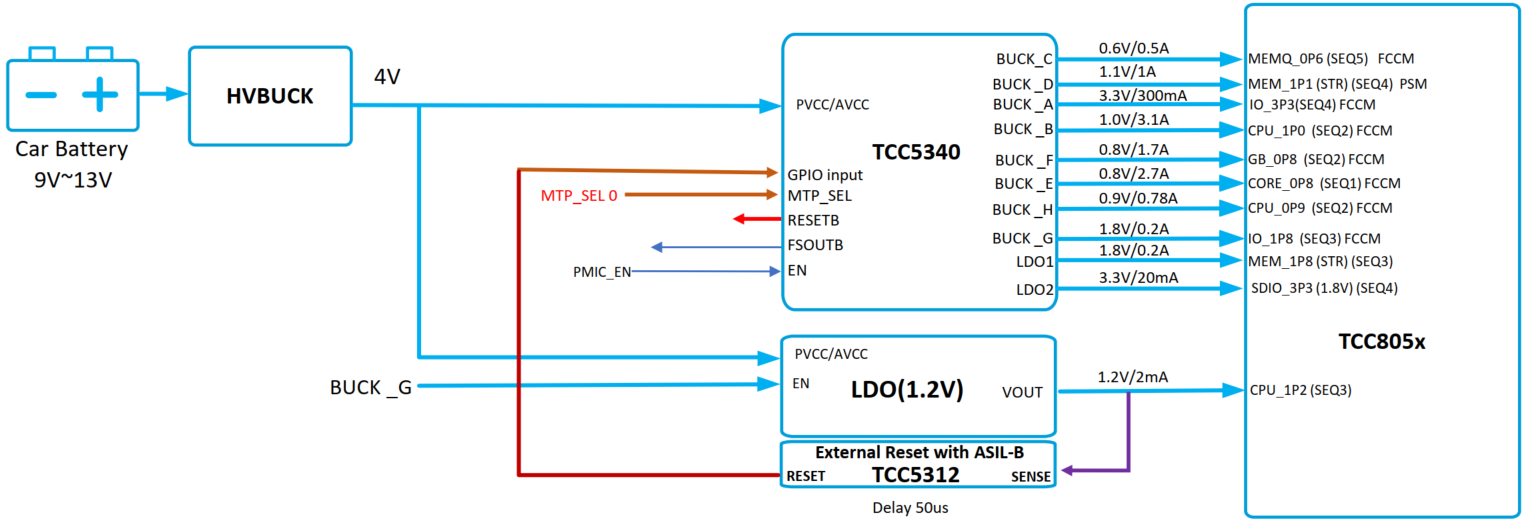


Figure . Block Diagram of PMICs Power Circuit

## Design Guide for Preventing IR Drop

IR drop refers to a voltage drop that appears at the resistive component of any impedance.

IR drop is the electrical potential difference between the two ends of a conducting phase during a current flow.

Depending on the environment of the PCB, an IR drop may occur.

If an IR drop occurs, you should increase and supply the voltage according to “*TCC805x Full Specification*”. [2]

Telechips PMICs have an I2C control function. If necessary, the voltage can be changed by using I2C.

### TCC5340

The TCC5340 is used in both LPDDR4 and LPDDR4X circuits. Figure 2.4 shows the power configuration of TCC5340.

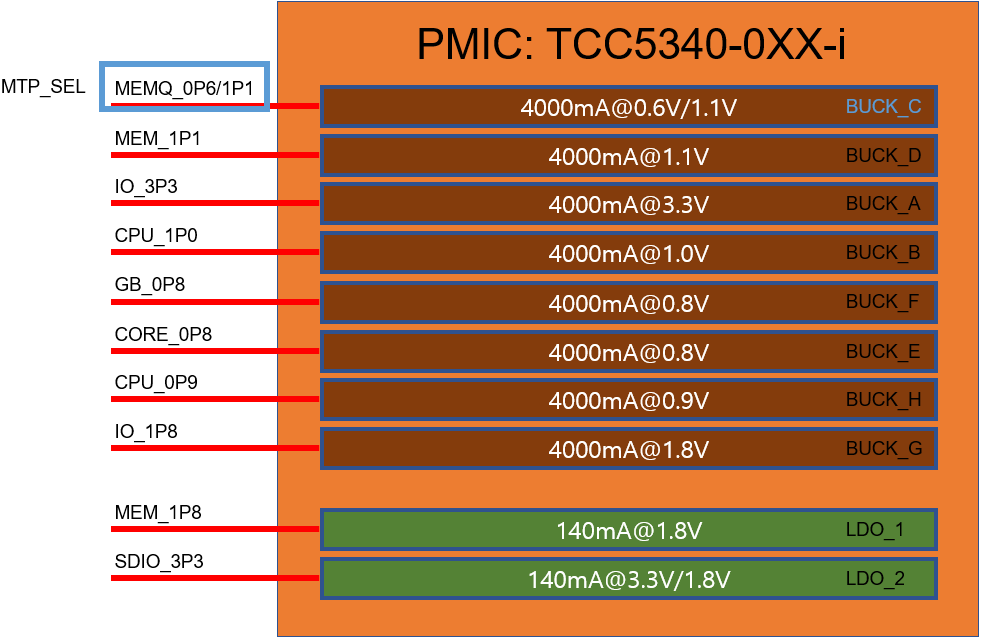


Figure . Power Configuration of TCC5340

Depending on the MTP\_SEL selection, the voltage of the BUCK\_C channel changes.

Table . MTP\_SEL Description of TCC5340

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Status** | **Voltage** | **Application** |
| MTP\_SEL | HIGH | 1.1V | LPDDR4 |
| MTP\_SEL | LOW | 0.6V | LPDDR4X |

## Power on and off Sequence

### Transistor Circuit for Power on and off Control

**Power on sequence**

1. **PWR\_CTLA** and **PWR\_CTLB** are controlled by TCC805x when the power is turned on or waken up.
2. **PWR\_EN** is logically high.
3. **HVBUCKEN** is logically high by **PWR\_EN**: High with OR logic. (PWR\_EN: High OR PMIC\_HVBUCKEN: Low= High)
4. The high voltage buck is turned on.
5. PMIC is turned on and **PMIC\_HVBUCKEN** is logically High.
6. The system is turned on.
7. **SYS\_PWR\_EN** is logically high and the peripheral device is turned on.

**Power off sequence**

1. **PWR\_CTLA** and **PWR\_CTLB** are controlled by TCC805x at the time of power off or power-down.
2. **PWR\_EN** is logically low.
3. PMIC detects **PMIC\_SYS\_EN**: Low by **PWR\_EN**.
4. PMIC processes power off sequence. At this time, the **PMIC\_HVBUCKEN** pin is high, so the status of the high voltage buck can be kept as ON.
5. **SYS\_PWR\_EN** is logically low and the peripheral device is turned off.
6. **HVBUCKEN** is logically low by **PMIC\_HVBUCKEN**: Low with OR logic. (PWR\_EN: Low OR PMIC\_HVBUCKEN: Low= Low)
7. The high voltage buck is turned off, and then the system goes into power off or power-down status.

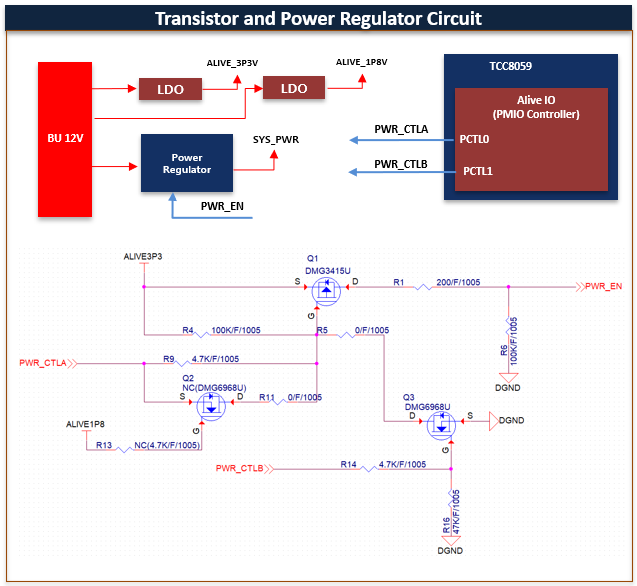


Figure . Transistor and Power Regulator Circuit

Table . Truth Table for Transistor Circuit

|  |  |  |  |
| --- | --- | --- | --- |
| PWR\_CTLA | PWR\_CTLB | PWR\_EN | SYS\_PWR |
| Low (0) | Low (0) | High (1) | ON |
| Low (0) | High (1) | High (1) | ON |
| High (1) | Low (0) | Low (0) | OFF |
| High (1) | High (1) | High (1) | ON |

### Power on Sequence of PMIC and External LDO

1. **PWR\_EN** is logically high.
2. **HVBUCKEN** is logically high.
3. **TCC5340** is turned on.
   1. PMIC\_BUCK\_E On (CORE\_0P8)
   2. PMIC\_BUCK\_B On (CPU\_1P0)/ PMIC\_BUCK\_F On (GB\_0P8)/ PMIC\_BUCK\_H On (CPU\_0P9)
   3. PMIC\_BUCK\_G On (IO\_1P8)/ PMIC\_LDO1 On (MEM\_1P8)/ EXT\_LDO ON (CPU\_1P2)
   4. PMIC\_BUCK\_A On (IO\_3P3)/ PMIC\_BUCK\_D On (MEM\_1P1)/ PMIC\_LDO2 On (SDIO\_3P3)
   5. PMIC\_BUCK\_C On (MEMQ\_0P6 or \*MEMQ\_1P1)

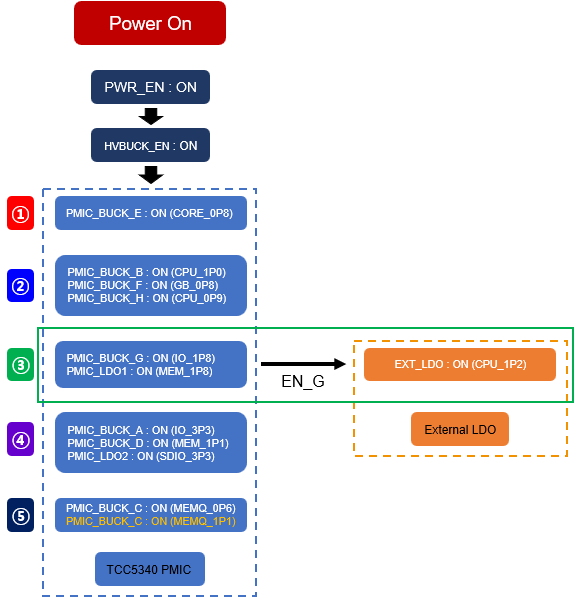


Figure . Power on Sequence Flowchart of PMIC and External LDO

### Power off Sequence of PMIC, External Buck, and External LDO

1. **PWR\_EN** is logically low.
2. **HVBUCKEN** is logically high.
3. **PMIC\_SYS\_EN** is logically low.
   1. PMIC\_BUCK\_C Off (MEMQ\_0P6 or \*MEMQ\_1P1)
   2. PMIC\_BUCK\_A Off (IO\_3P3)/ PMIC\_BUCK\_D Off (MEM\_1P1)/ PMIC\_LDO2 Off (SDIO\_3P3)
   3. PMIC\_BUCK\_G Off (IO\_1P8)/ PMIC\_LDO1 Off (MEM\_1P8)/ EXT\_LDO Off (CPU\_1P2)
   4. PMIC\_BUCK\_B Off (CPU\_1P0)/ PMIC\_BUCK\_F Off (GB\_0P8)/ PMIC\_BUCK\_H Off (CPU\_0P9
   5. PMIC\_BUCK\_E Off (CORE\_0P8)
   6. HVBUCKEN is logically low.

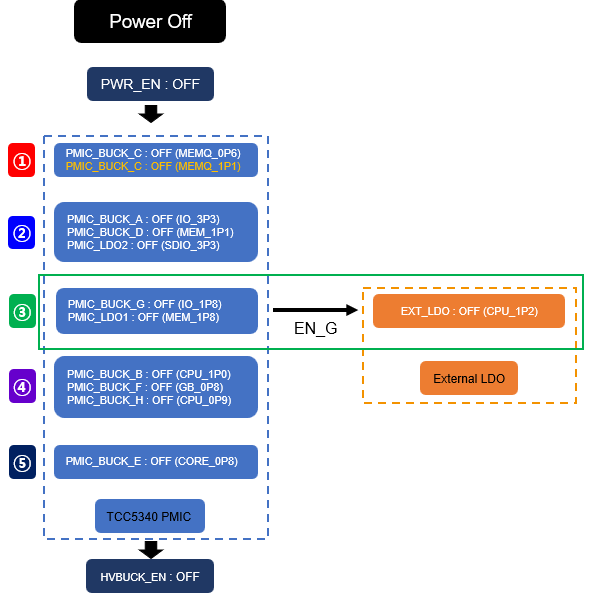


Figure . Power off Sequence Flowchart of PMIC and External LDO

\***Note:** In case use LPDDR4

## Power Rail

Table . Power Rail of Telechips PMIC Power Circuit

| PMIC Power Circuit | | | | | TCC8050/TCC8053 | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Power on Sequence | Power off Sequence | Power  Supply | Output Voltage  [V] | Maximum Output Current  [mA] | Power Name | MIN  Voltage  [V] | TYP  Voltage  [V] | MAX  Voltage  [V] |
| 1 | 5 | PMIC\_BUCK\_E  (CORE\_0P8) | 0.8 | 4000 | VDD08D\_CORE | 0.76 | 0.8 | 0.84 |
| VDD08A\_DPLL | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_GB | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_VB | 0.76 | 0.8 | 0.84 |
| VDD08A\_NPLL | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_MICOM | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_CA72 | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_CA53 | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_MB | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_PCIE | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_MIPI | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_DPWRAP | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_SDM | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_SRVC | 0.76 | 0.8 | 0.84 |
| VDD08A\_PLL\_STRGB | 0.76 | 0.8 | 0.84 |
| LVDS0\_P\_VDD | 0.76 | 0.8 | 0.84 |
| LVDS1\_P\_VDD | 0.76 | 0.8 | 0.84 |
| LVDS2\_P\_VDD | 0.76 | 0.8 | 0.88 |
| USB30\_VP | 0.76 | 0.8 | 0.84 |
| DP\_PHY\_VP08A | 0.76 | 0.8 | 0.84 |
| PCIE\_VDD | 0.76 | 0.8 | 0.84 |
| VDD08D\_DB | 0.76 | 0.8 | 0.84 |
| VDD08D\_VB | 0.76 | 0.8 | 0.84 |
| 2 | 4 | PMIC\_BUCK\_F  (GB\_0P8) | 0.8 | 4000 | VDD08D\_GB | 0.76 | 0.8 | 0.84 |
| 2 | 4 | PMIC\_BUCK\_B  (CPU\_1P0) | 1.0 | 4000 | VDD10D\_CPUA72 | 0.95 | 1.0 | 1.05 |
| 2 | 4 | PMIC\_BUCK\_H  (CPU\_0P9) | 0.9 | 4000 | VDD09D\_CPUA53 | 0.855 | 0.9 | 0.945 |
| USB30\_DVDD | 0.84 | 0.9 | 0.99 |
| UFS\_VDD09A | 0.855 | 0.9 | 0.945 |
| UFS\_VDD09A\_CMN | 0.855 | 0.9 | 0.945 |
| VDD09D\_USB20H | 0.84 | 0.9 | 0.99 |
| VDD09D\_USB20DH | 0.84 | 0.9 | 0.99 |
| MS1\_VDD\_0P9 | 0.855 | 0.9 | 0.945 |
| MS0\_VDD\_0P9 | 0.855 | 0.9 | 0.945 |
| VDD09D\_DMC | 0.855 | 0.9 | 0.945 |
| VDD09A\_PLL\_DDR0 | 0.855 | 0.9 | 0.945 |
| VDD09A\_PLL\_DDR1 | 0.855 | 0.9 | 0.945 |
| VDD09A\_PLL\_DDR2 | 0.855 | 0.9 | 0.945 |
| VDD09A\_PLL\_DDR3 | 0.855 | 0.9 | 0.945 |
| 3 | 3 | PMIC\_BUCK\_G  (IO\_1P8) | 1.8 | 4000 | VDD18A\_DPLL | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_GB | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_VB | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_MB | 1.700 | 1.800 | 1.900 |
| VDD18A\_NPLL | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_MICOM | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_CA72 | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_CA53 | 1.700 | 1.800 | 1.900 |
| MS0\_VDD18 | 1.710 | 1.800 | 1.890 |
| MS1\_VDD18 | 1.710 | 1.800 | 1.890 |
| LVDS0\_P\_VDDIO18 | 1.710 | 1.800 | 1.890 |
| LVDS0\_P\_VDDPLL18 | 1.710 | 1.800 | 1.890 |
| LVDS1\_P\_VDDIO18 | 1.710 | 1.800 | 1.890 |
| LVDS1\_P\_VDDPLL18 | 1.710 | 1.800 | 1.890 |
| LVDS2\_P\_VDDIO18 | 1.710 | 1.800 | 1.890 |
| LVDS2\_P\_VDDPLL18 | 1.710 | 1.800 | 1.890 |
| USB30\_VDD18 | 1.680 | 1.800 | 1.980 |
| USB30\_VPH | 1.710 | 1.800 | 1.890 |
| VDD18A\_USB20H | 1.680 | 1.800 | 1.980 |
| VDD18A\_USB20DH | 1.680 | 1.800 | 1.980 |
| UFS\_VDD18A\_CMN | 1.710 | 1.800 | 1.890 |
| VDD18D\_UFS\_OSC | 1.710 | 1.800 | 1.890 |
| PCIE\_VDDH | 1.710 | 1.800 | 1.890 |
| DP\_PHY\_VPH18A | 1.710 | 1.800 | 1.890 |
| VDD18D\_DP\_OSC | 1.710 | 1.800 | 1.890 |
| DP\_AUX\_VPH18A | 1.710 | 1.800 | 1.890 |
| VDD18P\_IO | 1.650 | 1.800 | 1.950 |
| VDD18A\_ADC | 1.700 | 1.800 | 1.900 |
| VDD18A\_TS | 1.710 | 1.800 | 1.890 |
| VDD18P\_GPSYS | 1.650 | 1.800 | 1.950 |
| UFS\_VDD18A | 1.710 | 1.800 | 1.890 |
| VDD18D\_MAIN\_OSC | 1.710 | 1.800 | 1.890 |
| VDD18A\_PLL\_PCIE | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_MIPI | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_DDR0 | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_DDR1 | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_DDR2 | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_DDR3 | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_DPWRAP | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_SDM | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_SRVC | 1.700 | 1.800 | 1.900 |
| VDD18A\_PLL\_STRGB | 1.700 | 1.800 | 1.900 |
| VDD18D\_GPSD0 | 1.650 | 1.800 | 1.950 |
| eMMC (VCCQ) | 1.650 | 1.800 | 3.600 |
| 3 | 3 | PMIC\_LDO\_1  (MEM\_1P8) | 1.8 | 140 | DRAM\_VDD1 | 1.700 | 1.800 | 1.950 |
| 3 | 3 | EXT\_LDO  (MIPI\_1P2) | 1.2 | 140 | M1\_VDD12 | 1.14 | 1.2 | 1.26 |
| M0\_VDD12 | 1.14 | 1.2 | 1.26 |
| VDD12D\_UFS | 1.08 | 1.2 | 1.32 |
| 4 | 2 | PMIC\_BUCK\_A  (IO\_3P3) | 3.3 | 4000 | USB30\_VDD33 | 3.070 | 3.300 | 3.600 |
| VDD33A\_USB20H | 3.070 | 3.300 | 3.600 |
| VDD33A\_USB20DH | 3.070 | 3.300 | 3.600 |
| VDD33D\_GPSD2 | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPA | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPB | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPC | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPE | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPG | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPH | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPMA | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPMB | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPMC | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPMD | 3.000 | 3.300 | 3.600 |
| VDD33D\_GPSYS | 3.000 | 3.300 | 3.600 |
| SNOR (VCC) | 2.700 | 3.300 | 3.600 |
| eMMC (VCC) | 2.700 | 3.300 | 3.600 |
| 4 | 2 | PMIC\_LDO\_2  (SDIO\_3P3) | 3.3 | 140 | VDD33D\_GPSD1 | 3.000 | 3.300 | 3.600 |
| 4 | 2 | PMIC\_BUCK\_D  (MEM\_1P1) | 1.1 | 4000 | DRAM0\_VDDQ\_CKE | 1.060 | 1.100 | 1.170 |
| DRAM1\_VDDQ\_CKE | 1.060 | 1.100 | 1.170 |
| LPDDR4\_VDD2 | 1.060 | 1.100 | 1.170 |
| 5 | 1 | PMIC\_BUCK\_C  (MEMQ\_0P6) | 0.6 | 4000 | LPDDR4\_VDDQ | 0.570 | 0.6 | 0.630 |
| 5 | 1 | \*PMIC\_BUCK\_C  (MEMQ\_1P1) | 1.1 | 4000 | LPDDR4\_VDDQ | 1.060 | 1.100 | 1.170 |

\***Note:** In case use LPDDR4.

# Power-on and off Sequence

## Power-on/off Sequence Timing of PMIC

Figure 3.1 shows the power-on sequence timing of PMIC.

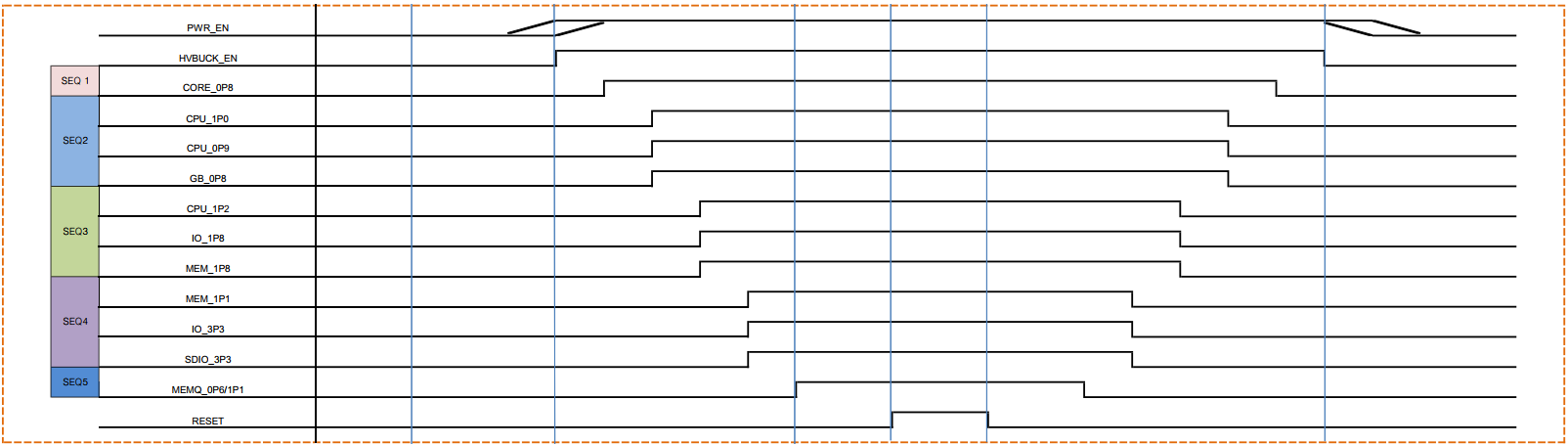


Figure . Power-on/off Sequence Timing of PMIC

The power sequence is determined by the internal OTP settings of PMICs. For detailed OTP information on PMIC, contact Telechips. [1]

## Power on Waveform(TBD)

## Power off Waveform(TBD)

# References

1. Contact Telechips for more details: [sales@telechips.com](mailto:auto_sales@telechips.com)
2. TCC805x Full Specification

**Note**: Reference documents can be provided whenever available, depending on the terms of a contract. If the reference

documents are unavailable, the contents directly related to your development can be guided.

# Revision History

## Rev. 0.10: 2025-03-19

* Preliminary version release

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